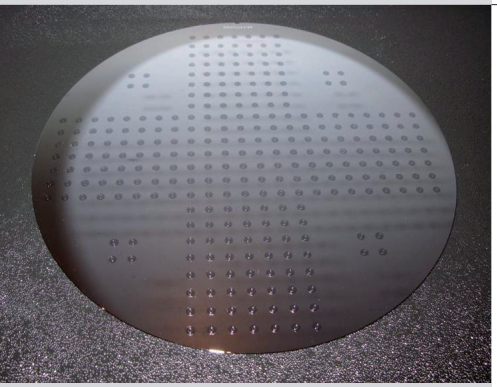
PROJECT RESULT

Lithography

## 2T305: Full assessment of nano-imprint technology addressing sub-35 nm ICs (FANTASTIC)



# Assessing nanoimprint lithography for CMOS

**UV nanoimprint technology has been seen as a competitive candidate for use in the next generation of lithographic processes due to the advantages offered in terms of resolution and cost, particularly for chip manufacture at the 32 nm node and beyond. The MEDEA+ FANTASTIC project assessed its suitability for production use, particularly for CMOS applications. While the technology is not yet capable of the cost efficiency needed for CMOS production, it shows promise for several new manufacturing applications. The outcome of the project has been issued as guidance for others developing the technology.**

The most common method of transferring the geometric pattern of the layer of an integrated circuit to the substrate is by optical lithography. This lithographic stage is a key component of the semiconductor manufacturing process. It is a highly laborious one however; for a complex CMOS integrated circuit the wafer may have to undergo the photolithographic cycle as much as 50 times.

In the constant search for technology improvements that can save costs, one potentially interesting alternative is the use of ultra-violet (UV) nanoimprint lithography. This method makes use of a stamp material – typically silicon or quartz – with a pattern produced by electron-beam (e-beam) lithography. The stamp is then physically pressed against a substrate coated with a UV-curable low-viscosity resist, thus transferring the desired circuit pattern to the substrate in a one-shot process.

The substrate is hardened by shining UV light through it. At this point, the stamp is removed, leaving a three-dimensional imprint of the circuit in place on the substrate. This ability to apply a 3D pattern to a substrate in a single process is seen as another major advantage of UV nanoimprint lithography.

## Added to the ITRS roadmap

Nanoimprint lithography technology was accordingly added to the international semiconductor technology roadmap (ITRS) in 2003 as a potentially useful method of assisting in microelectronics manufacturing at the 32 nm node and below. However, the microelectronics industry hesitated to apply the technique as there was a significant lack of data on the necessary tools, template fabrication, measurement methods and other aspects. Participants in the MEDEA+ 2T305 FANTASTIC project therefore undertook to develop and assess the suitability of UV nanoimprint lithography for production use, in particular for advanced CMOS applications.

The project partners began by carrying out a detailed assessment of the UV nanoimprint process itself, including technological ability, required effort to develop production solutions and the cost of ownership. FANTASTIC investigated all aspects of the technology involved: the manufacturing tools, the imprint process, template fabrication – including patterning, inspection and repair – and process integration.

FANTASTIC was driven by the leading European semiconductor design and manufacturing companies. Project partners also included major production equipment suppliers, mask-making shops and key microelectronics research institutes engaged in nanoimprint activities. Their objective was to demonstrate the potential of UV nanoimprint technology for CMOS applications at the sub-50 nm level.

If successful, a follow-up project would establish the full infrastructure for volume production at 32 nm.

## Technology lacks maturity

However, by the end of the project, the FANTASTIC partners were forced to conclude that the UV nanoimprint lithographic process was not suited to CMOS production at 32 nm node levels and below. This was largely due the high level of mould defects resulting from the direct-contact phase of the process.

Another issue was the fact that mask design had to be carried out at a one-to-one ratio, rather than the four-to-one reduction more usual with optical lithographic methods. Lithographic patterns are written on the stamp using an electron beam with the same line width as that of the pattern on the wafer, rather than reducing it by four times as with conventional optical lithography. This handicap placed very high demands on the mask-design process.

After a thorough analysis of the project results therefore, the project team came to the conclusion that the technology is not yet mature enough to replace existing CMOS production methods at the 32 nm node. However, several of the partners developed their expertise levels within the project to the point where they are now competing successfully in new global markets.

Moreover, the MEDEA+ project did successfully demonstrate that UV nanoimprint lithography could be of benefit to emerging production applications even if this technology is not suitable for very advanced CMOS technologies.

Some partners for example have developed design and manufacturing expertise in the microfabrication of lenses, in the production of photovoltaic applications and in light-emitting diodes (LEDs), radio-frequency identification (RFID) and biotechnology. All these applications require less aggressive high-resolution lithography. Moreover, such applications represent world markets that are relatively recent and are growing rapidly.

Regarding equipment advances, a complete step-and-repeat tool – EVG 770 – was developed and built within the scope of the FANTASTIC project and Merit HR 32, a new 32 nm mask repair tool based on e-beam technology, was successfully introduced at Semicon Japan 2009.

## Clear guidance issued

Early access to advanced lithography technology is vital for European competitiveness in chipmaking. Manufacturing technologies for high-volume production of nanoelectronics devices have to be fast, low cost and – above all – reliable.

UV nanoimprint lithography – despite the limitations identified in terms of defects when used for advanced CMOS processes – has demonstrated many other possibilities for manufacturing applications for existing and future lithography options.

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**KEY PROJECT DATES:**

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